The Pending Claims:

Claim 1(previously presented):

A method of surface pretreatment before selective epitaxial growth process, comprising:

providing a semiconductor substrate having a gate oxide layer thereon, a gate electrode on said gate oxide layer, a lightly doped drain region, a source region and a drain region therein;

forming an offset spacer around said gate oxide layer and said gate electrode;

tilting and implanting said semiconductor substrate with a predetermined angle to form a pocket region on the interface of the lightly doped drain region, said source and drain regions and said semiconductor substrate and under said lightly doped drain region without surrounding said lightly doped drain region, wherein a dosage of said pocket region is less than that of said lightly doped drain region;

performing a dry etching process with a carbon-free plasma source to remove a portion of said semiconductor substrate; and

performing a selective epitaxial growth process to form a semiconductor layer on said gate electrode, said source and drain regions for a salicide process.

Claim 2(original):

The method of claim 1, wherein said dry etching process is performed with a carbon-free plasma source containing hexaflorosulfur (SF_6) diluted with ambient gas.

Claim 3(original):

The method of claim 2, wherein said dry etching process is performed with a carbon-free plasma source containing hexaflorosulfur (SF_6) diluted with ambient gas selected from a group consisting of helium, neon, argon, hydrogen and nitrogen.

Claim 4(original):

The method of claim 2, wherein said dry etching process is performed with a carbon-free plasma source containing hexaflorosulfur (SF_6) having a volume ratio between about 0.5%and 5%.

Claim 5(original):

The method of claim 3, wherein said dry etching process is performed with a carbon-free plasma source containing hexaflorosulfur (SF_6) having a volume ratio between about 0.5%and 5%.

Claim 6(original):

The method of claim 4, wherein said dry etching process is performed at a pressure about 10 mtorr and a power between about 20 watts to about 500 watts, and an etching time within about 1 minutes.

Claim 7(original):

The method of claim 5, wherein said dry etching process is performed at a pressure about 10 mtorr and a power between about 20 watts to about 500 watts, and an etching time within about 1 minutes.

Claim 8(original):

The method of claim 1, wherein said dry etching process is performed to remove said semiconductor substrate about 20-50 angstroms.

Claim 9(original):

The method of claim 2, wherein said dry etching process is performed to remove said semiconductor substrate about 20-50 angstroms.

Claim 10(original):

The method of claim 1, wherein further comprising a baking process performed with hydrogen ambient gas at a temperature less than 750□ prior to said selective epitaxial growth process.

Claim 11(previously presented):

A method of forming a semiconductor device using selective epitaxial growth, comprising:

providing a semiconductor substrate with a first conductivity;

forming a plurality of isolation regions on said semiconductor substrate;

sequentially forming a gate dielectric layer and a gate electrode on said semiconductor substrate between each pair of said isolation regions;

forming a lightly doped drain region with a second conductivity opposite to said first conductivity in said semiconductor substrate between said gate electrode and each said isolation region;

forming a first spacer around said gate dielectric layer and said gate electrode;

forming a source/drain region with said second conductivity beside said lightly doped drain region in said semiconductor substrate;

tilting and implanting said semiconductor substrate with a predetermined angle to form a pocket region with said first conductivity on the interface of said lightly doped drain region, said source and drain regions and said semiconductor substrate and under said lightly doped drain region without surrounding said lightly doped drain region, wherein a dosage of said pocket region is less than that of said lightly doped drain region;

performing a dry etching process with a carbon-free plasma source to remove a portion of said semiconductor substrate;

performing a selective epitaxial growth process to form a semiconductor layer on said gate electrode, said source and drain regions;

forming a metal layer on said semiconductor layer; and

performing a salicide process to form a silicide layer on said gate_electrode, said source and drain regions.

Claim 12(original):

The method of claim 11, wherein said dry etching process is performed with a carbon-free plasma source containing hexaflorosulfur (SF_6) diluted with ambient gas.

Claim 13(original):

The method of claim 12, wherein said dry etching process is performed with a carbon-free plasma source containing hexaflorosulfur (SF_6) diluted with ambient gas selected from a group consisting of helium, neon, argon, hydrogen and nitrogen.

Claim 14(original):

The method of claim 12, wherein said dry etching process is performed with a carbon-free plasma source containing hexaflorosulfur (SF_6) having a volume ratio between about 0.5%and 5%.

Claim 15(original):

The method of claim 13, wherein said dry etching process is performed with a carbon-free plasma source containing hexaflorosulfur (SF_6) having a volume ratio between about 0.5%and 5%.

Claim 16(original):

The method of claim 14, wherein said dry etching process is performed at a pressure about 10 mtorr and a power between about 20 watts to about 500 watts, and an etching time within about 1 minutes.

Claim 17(original):

The method of claim 15, wherein said dry etching process is performed at a pressure about 10 mtorr and a power between about 20 watts to about 500 watts, and an etching time within about 1 minutes.

Claim 18(original):

The method of claim 11, wherein further comprising a baking process performed with hydrogen ambient gas at a temperature less than 750□ prior to said selective epitaxial growth process.

Claim 19(original):

The method of claim 11, wherein further comprising a step of forming a second spacer around said gate dielectric layer and said gate electrode prior to forming said first spacer.

Claim 20(original):

The method of claim 11, wherein said metal layer is selected from a group cons